Customer No.: 31561
Application No.: 10/710,933
Docket No.: 11537-US-PA

AMENDMENT

To the Claims:

Claim 1. (currently amended) A quad flat no-lead package structure, comprising:

a chip carrier having a top surface and a bottom surface, wherein a plurality of conductive leads is inlaid in the chip carrier and lower surfaces of the conductive leads are exposed by ~~disposed on~~ the bottom surface of the chip carrier, while a plurality of pads is disposed on the top surface of the chip carrier, the conductive leads being electrically connected to the pads; and

at least a chip, disposed on the top surface of the chip carrier and electrically connected to the chip carrier~~, wherein the chip covers at least a portion of the pads on the top surface of the chip carrier~~.

Claim 2. (original) The package structure as claimed in claim 1, further comprising a passivation layer to cover the chip.

Claim 3. (original) The package structure as claimed in claim 1, wherein the chip carrier includes an interconnect layer between the pads and the conductive leads, and wherein the interconnect layer includes at least a via for connecting one of the pads and one of the conductive leads.

Claim 4. **(cancelled)**.

Claim5. (original) The package structure as claimed in claim 1, wherein the chip is electrically connected to the chip carrier through flip chip technology.

Claim 6. (original) The package structure as claimed in claim 1, wherein the chip

is electrically connected to the chip carrier through surface mount technology.

Claim 7. (original) The package structure as claimed in claim 6, wherein an anisotropic conductive paste is further included to attach the chip and the chip carrier.

Claims 8-15 **(cancelled)**

Claim 16. (currently amended) A wafer-level package structure, comprising:

a silicon wafer, having a plurality of sections;

a plurality of conductive blocks, disposed on the silicon wafer and in each of the sections of the silicon wafer;

a metal interconnect layer, connecting the plurality of the conductive blocks, wherein the metal interconnect layer comprises at least a via hole and a plurality of pads, wherein the via hole electrically connects one of the conductive blocks and one of the pads, and wherein the pads are disposed on an uppermost surface of the metal interconnect layer; and

at least a chip, disposed onto each of the sections of the silicon wafer, wherein the chip includes a plurality of bonding pads that are correspondingly connected to the pads.

Claim 17. (original) The wafer-level package structure of claim 16, further comprising a passivation layer covering each section of the wafer.

Claim 18. (original) The wafer-level package structure of claim 16, wherein the metal interconnect layer further includes an oxide layer between the conductive blocks and the pads, while the via hole through the oxide layer connects one of the conductive blocks and one of the pads.

Claims 19-26 **(cancelled)**

Claim 27. (New) The package structure as claimed in claim 1, wherein all the pads are covered by at least the chip.